Fig. 1A FORMING STEP OF SILICON NITRIDE OXIDE FILM ($SiN_xB_yO_z$) 103a BY SPUTTERING

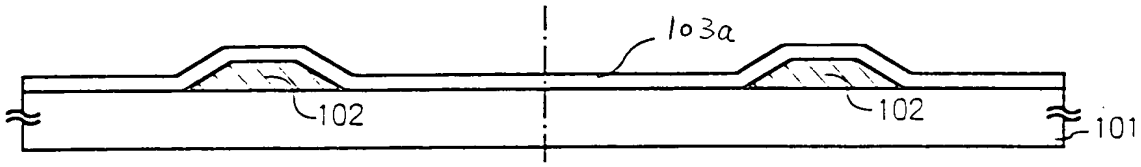


Fig. 1B FORMING STEP OF INSULATING FILM 103b AND SEMICONDUCTOR FILM

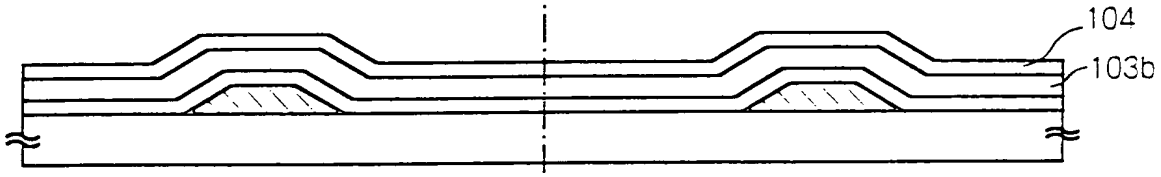


Fig. 1C LASER CRYSTALLIZATION STEP

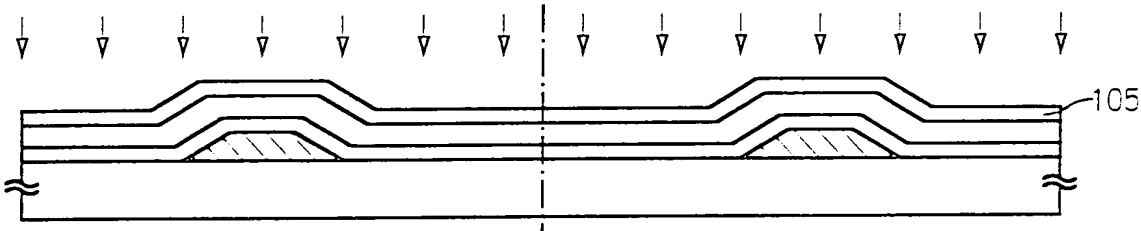


Fig. 1D BACK EXPOSURE STEP

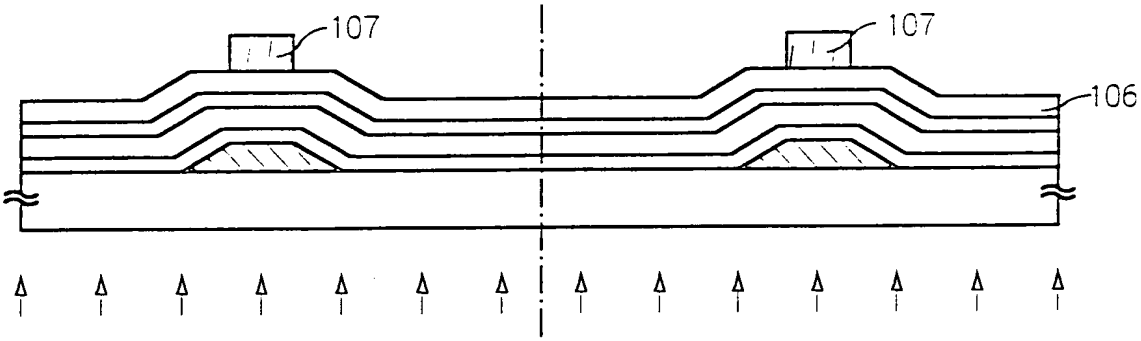


Fig. 1E ETCHING STEP

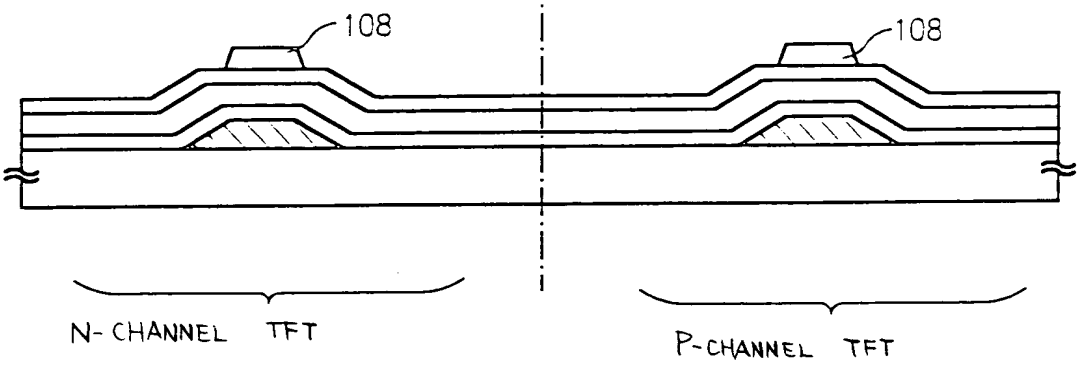


Fig. 2A DOPING STEP (FORMING STEP OF n^+ REGION)

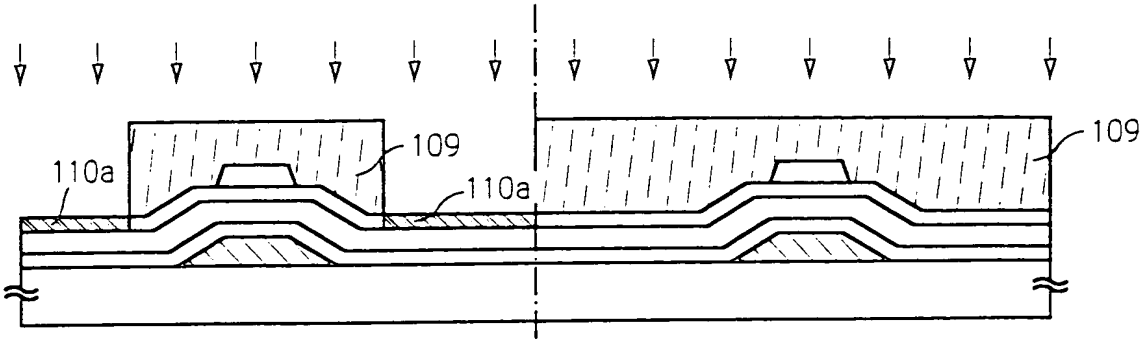


Fig. 2B FORMING STEP OF INSULATING FILM 111

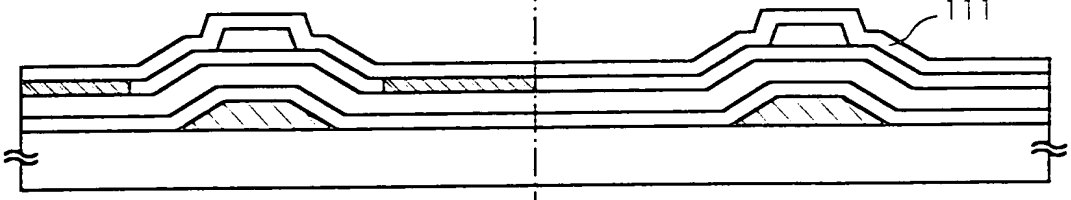


Fig. 2C DOPING STEP (FORMING STEP OF n^- REGION)

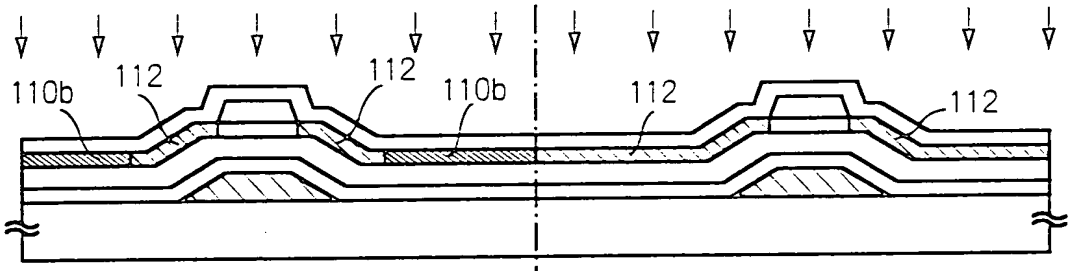
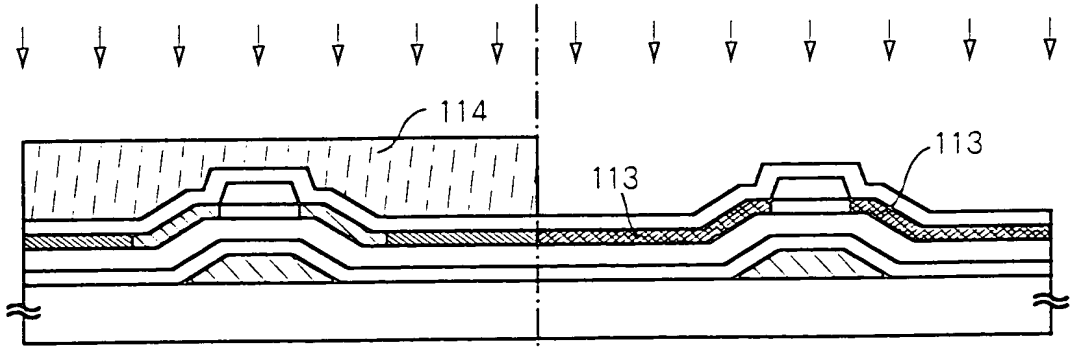


Fig. 2D DOPING STEP (FORMING STEP OF P^+ REGION)



N-CHANNEL TYPE TFT

P-CHANNEL TYPE TFT

Fig.3A ACTIVATION STEP

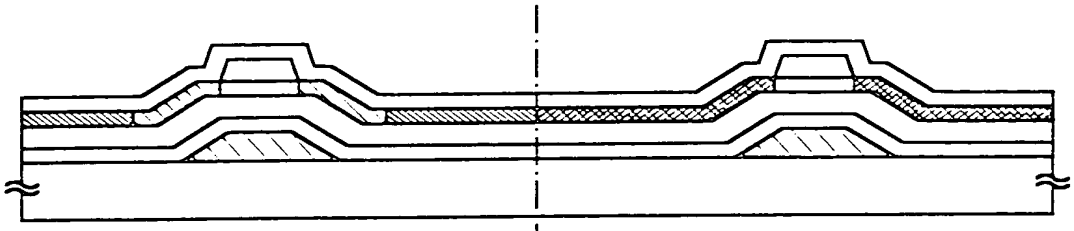


Fig.3B PATTERNING STEP

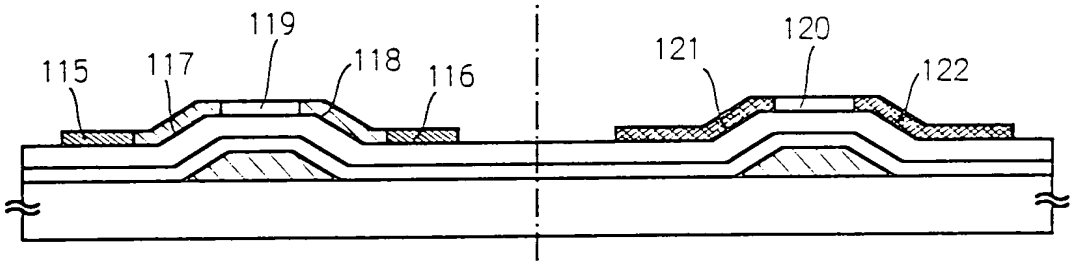


Fig.3C FORMING STEP OF INTERLAYER INSULATING FILM

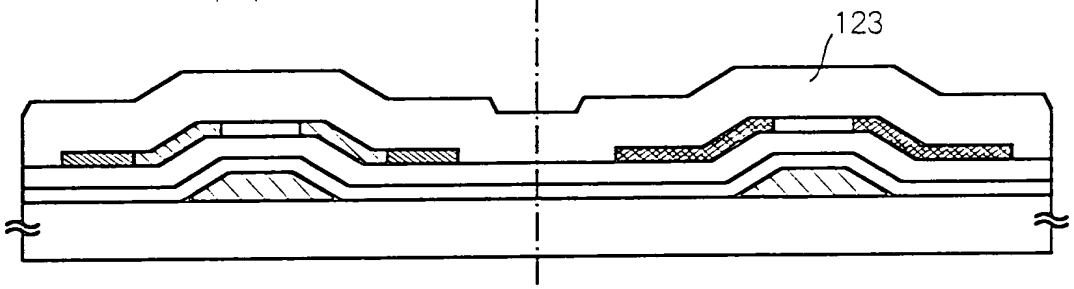


Fig.3D FORMING STEP OF SOURCE WIRING LINE AND DRAIN WIRING LINE

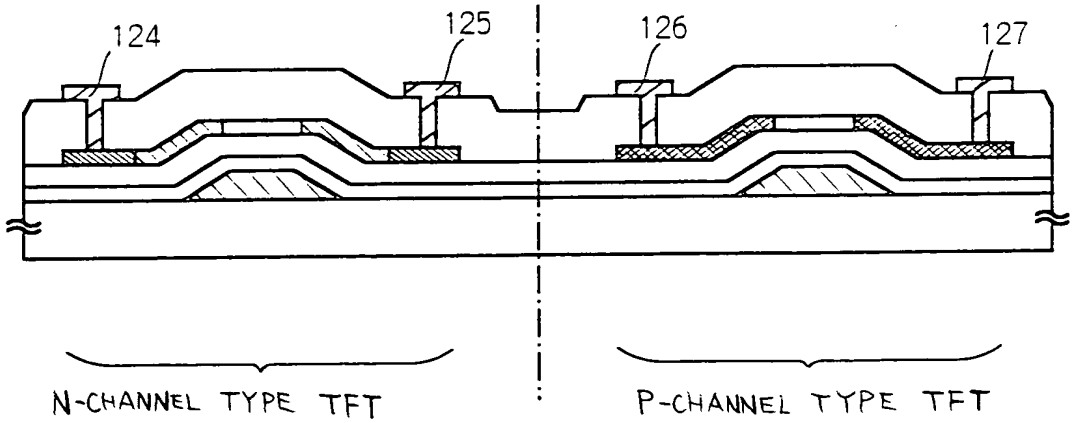


Fig.4A FORMING STEP OF SILICON NITRIDE OXIDE FILM ($SiN_xB_yO_z$) 103a BY SPUTTERING

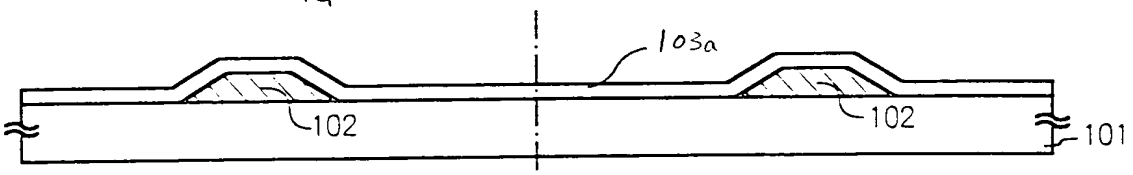


Fig.4B FORMING STEP OF INSULATING FILM 103b AND SEMICONDUCTOR FILM

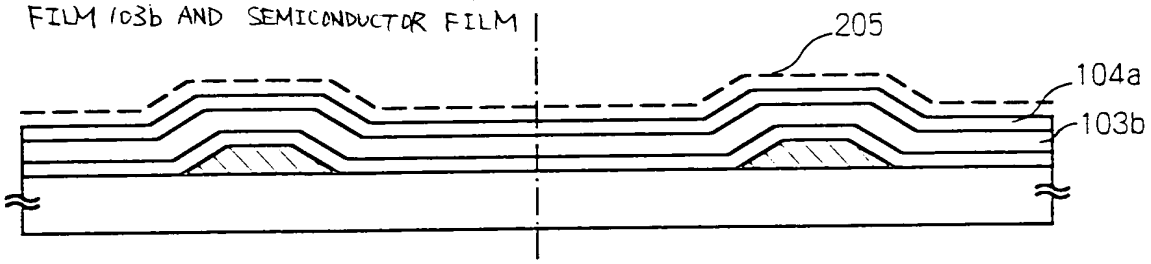


Fig.4C CRYSTALLIZING STEP BY HEAT TREATMENT

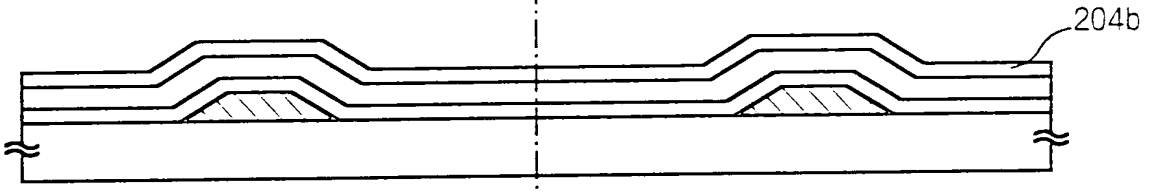


Fig.4D LASER IRRADIATION STEP

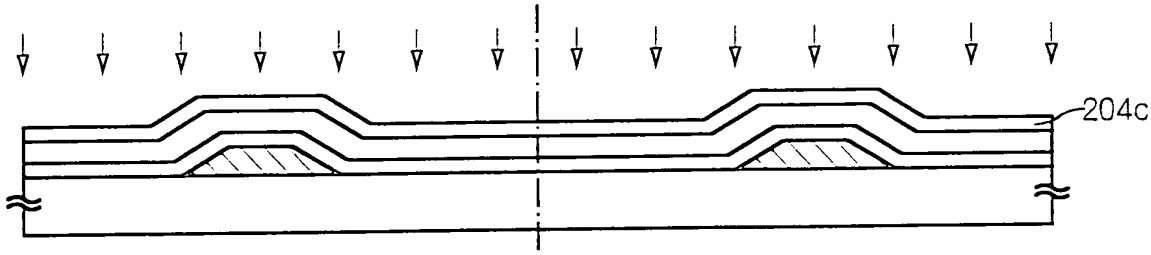


Fig.4E BACK EXPOSURE STEP

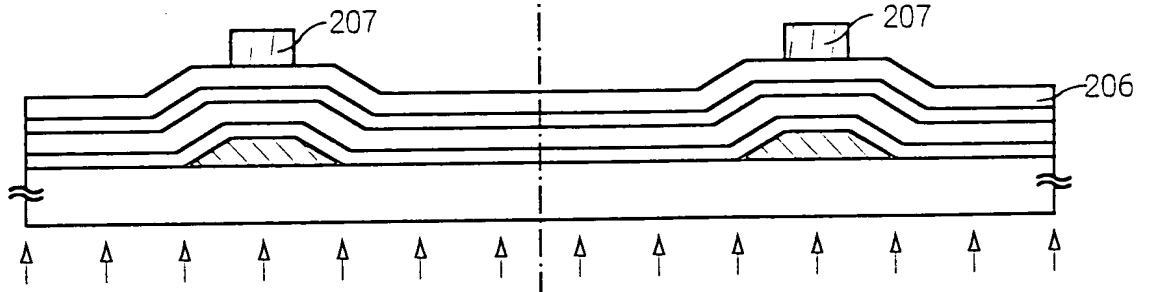


Fig.4F ETCHING STEP

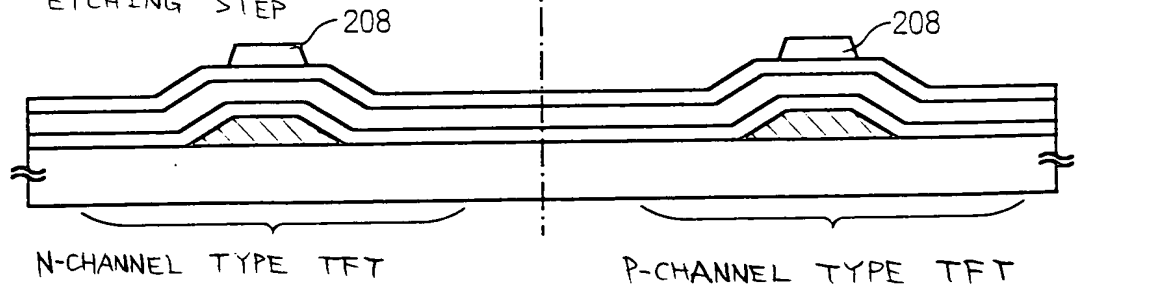


Fig.5A

DOPING STEP (FORMING STEP OF n^+ REGION)

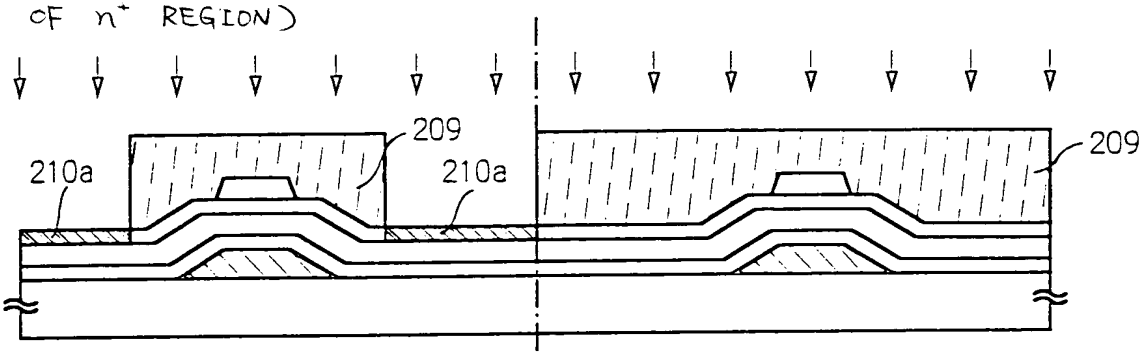


Fig.5B

FORMING STEP OF INSULATING FILM 211

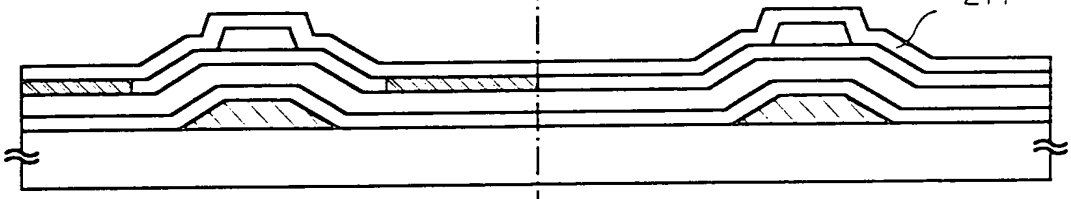


Fig.5C

DOPING STEP (FORMING STEP OF n^- REGION)

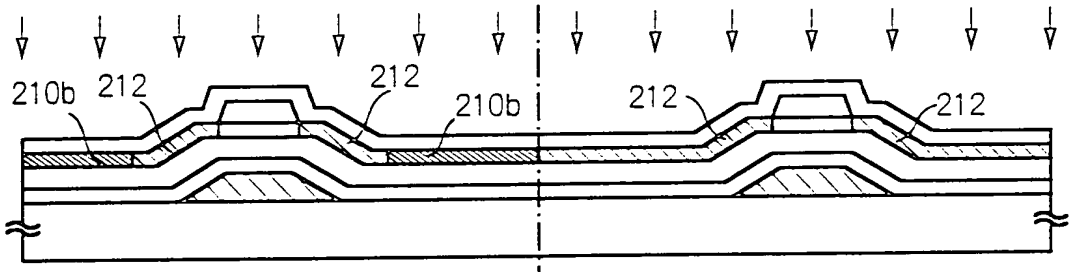
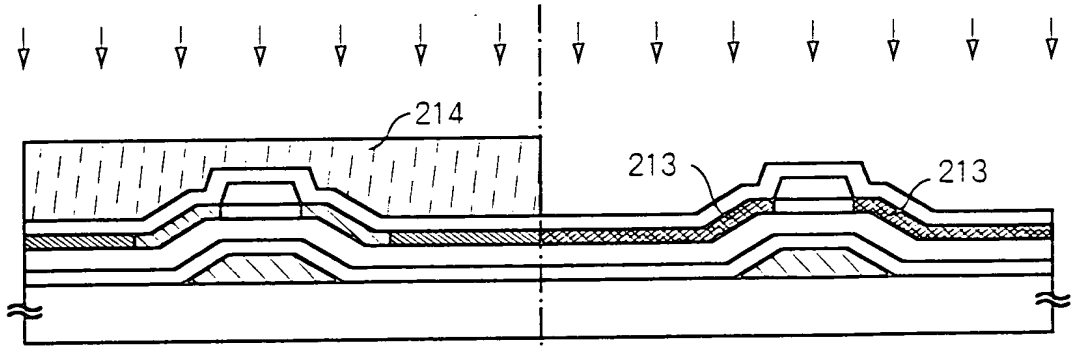


Fig.5D

DOPING STEP (FORMING STEP OF p^+ REGION)



N-CHANNEL TFT

P-CHANNEL TFT

Fig. 6A ACTIVATION AND GETTERING STEP

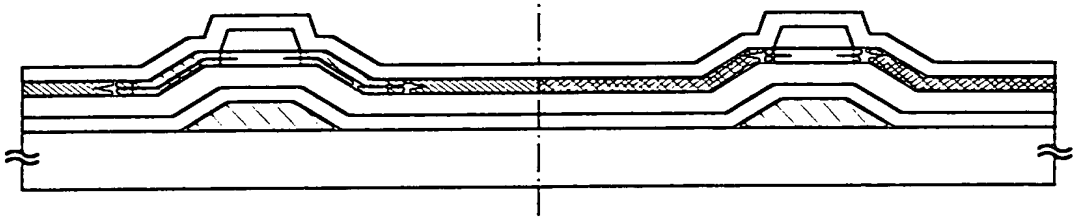


Fig. 6B PATTERNING STEP

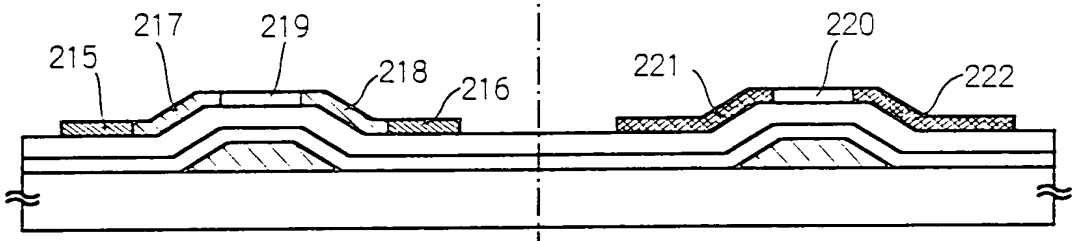


Fig. 6C FORMING STEP OF INTERLAYER INSULATING FILM

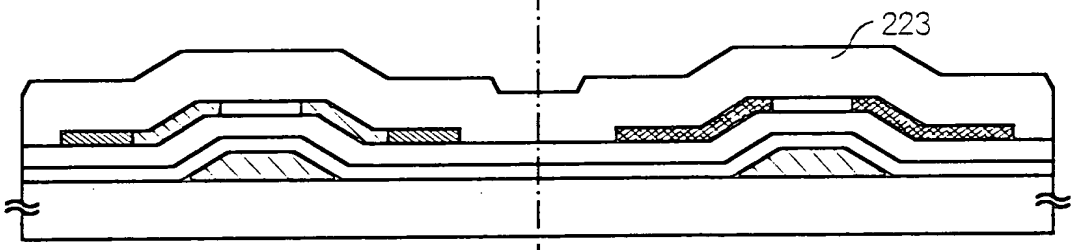
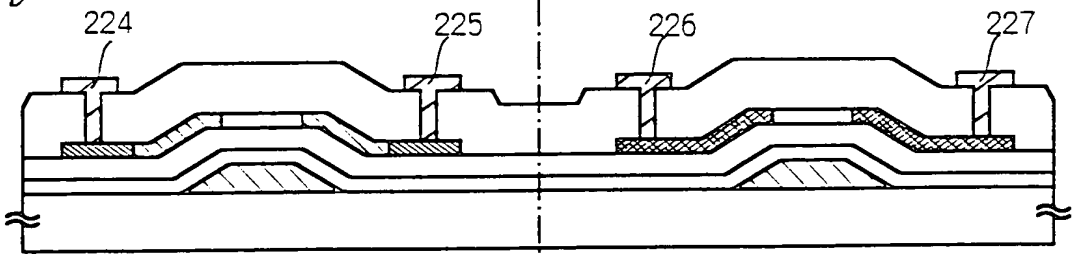


Fig. 6D FORMING STEP OF SOURCE WIRING LINE AND DRAIN WIRING LINE



N-CHANNEL TYPE TFT

P-CHANNEL TYPE TFT

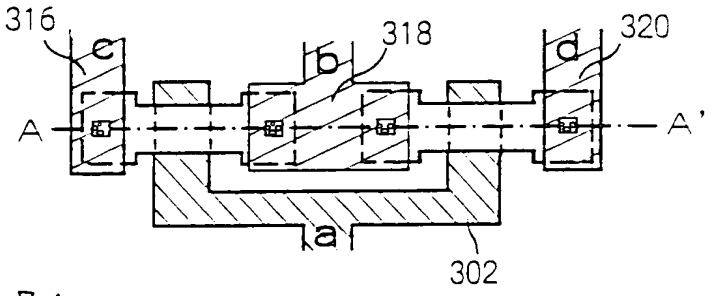


Fig. 7A TOP VIEW OF CMOS CIRCUIT

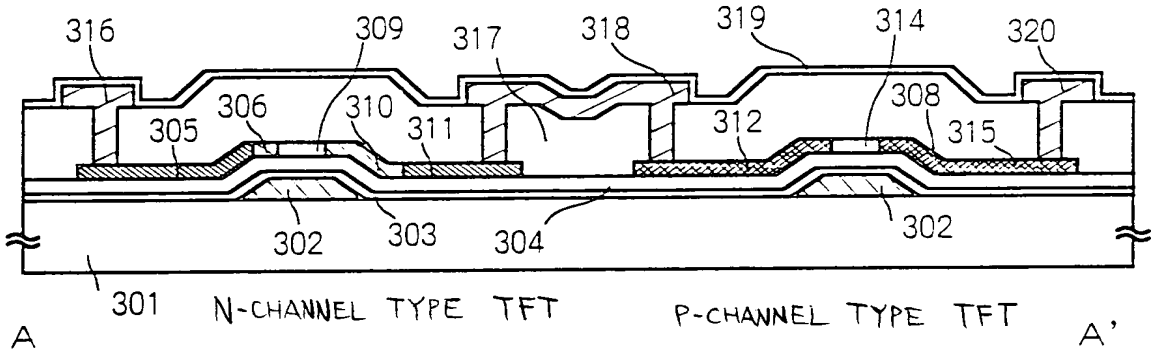


Fig. 7B SECTIONAL STRUCTURE VIEW ALONG A-A'

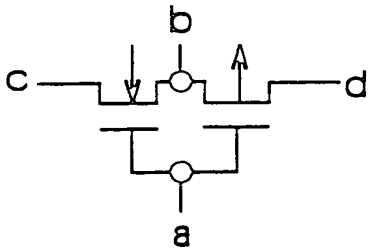


Fig. 7C CIRCUIT DIAGRAM OF CMOS

Fig. 8A TOP VIEW

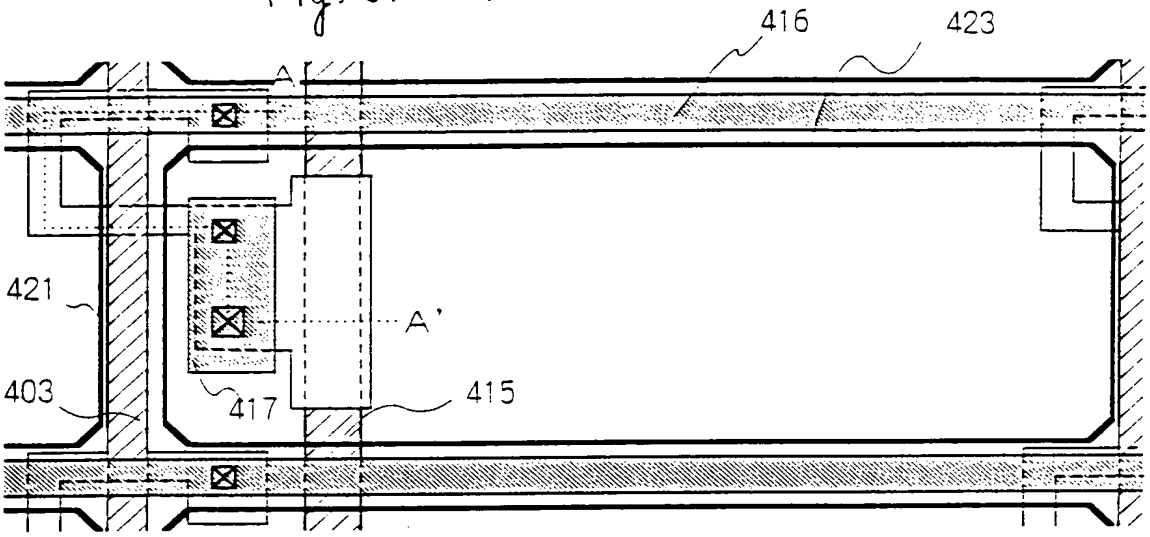
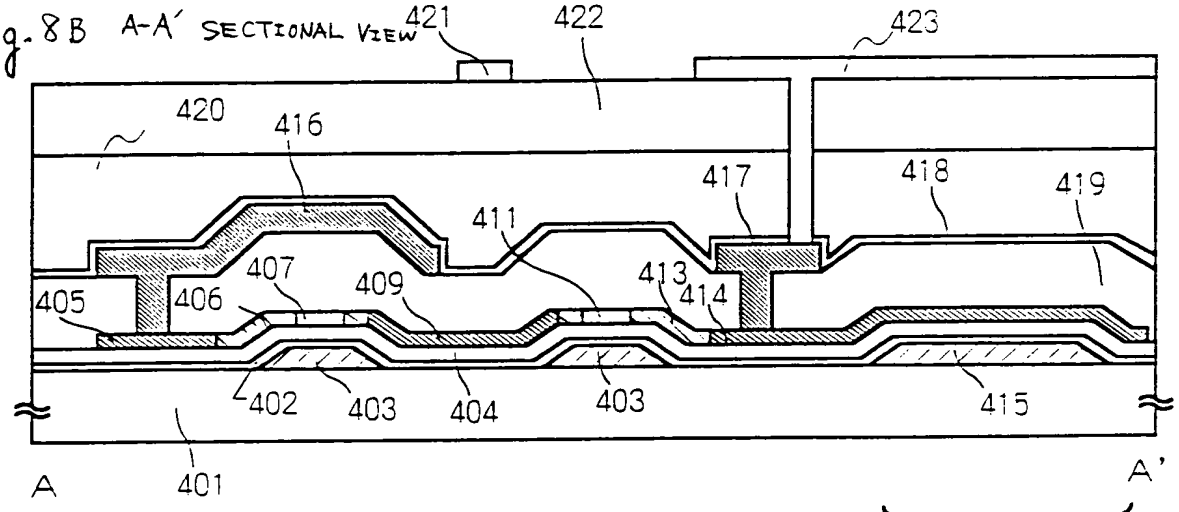


Fig. 8B A-A' SECTIONAL VIEW



PIXEL TFT PORTION

CAPACITANCE PORTION

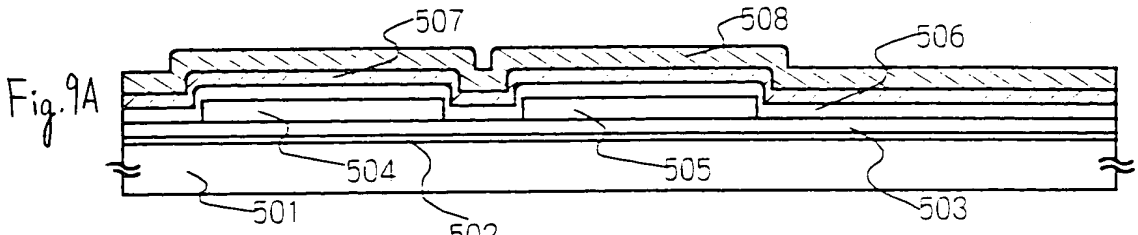


Fig. 9A

ADDITION OF IMPURITY TO GIVE N-TYPE (LOW CONCENTRATION)

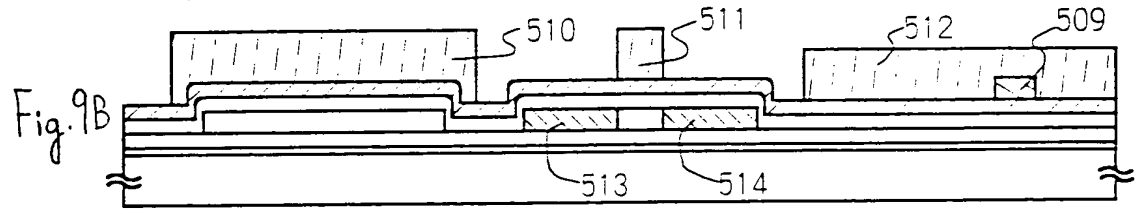


Fig. 9B

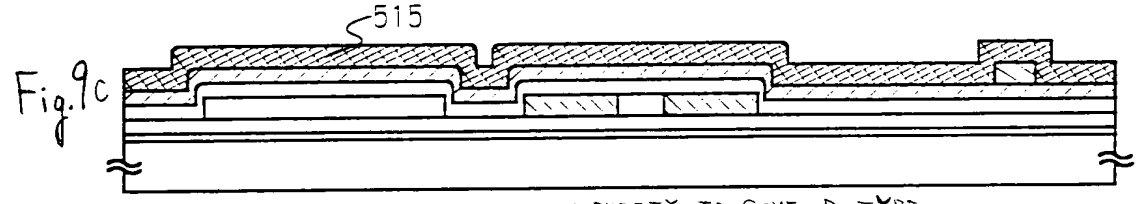


Fig. 9C

ADDITION OF IMPURITY TO GIVE P-TYPE (HIGH CONCENTRATION)

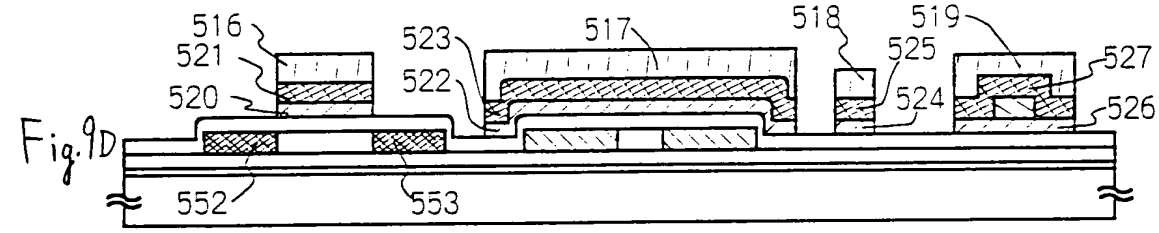


Fig. 9D

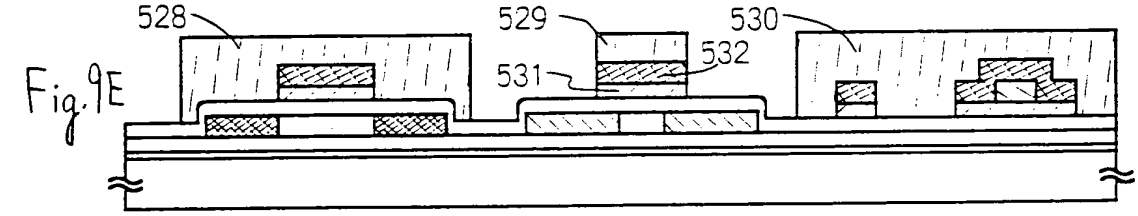


Fig. 9E

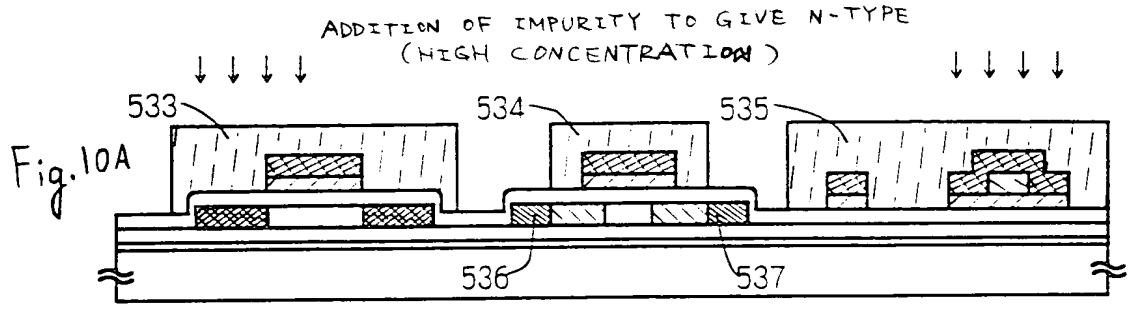


Fig.10A

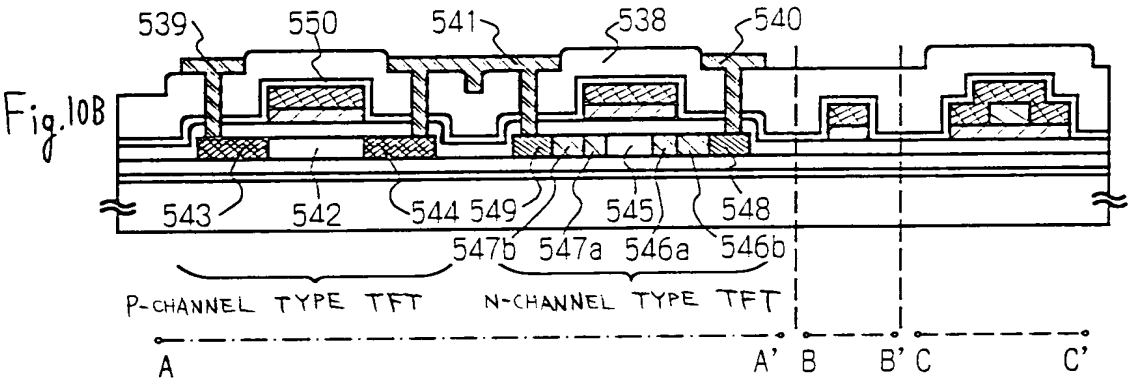


Fig.10B

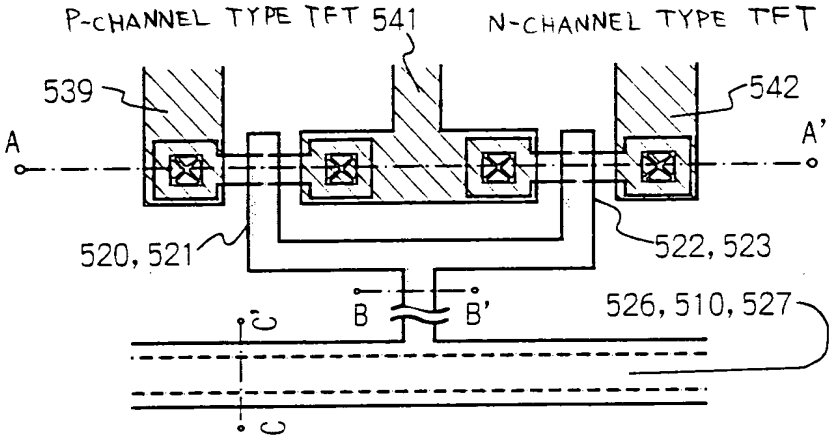


Fig.10C TOP VIEW OF CMOS CIRCUIT

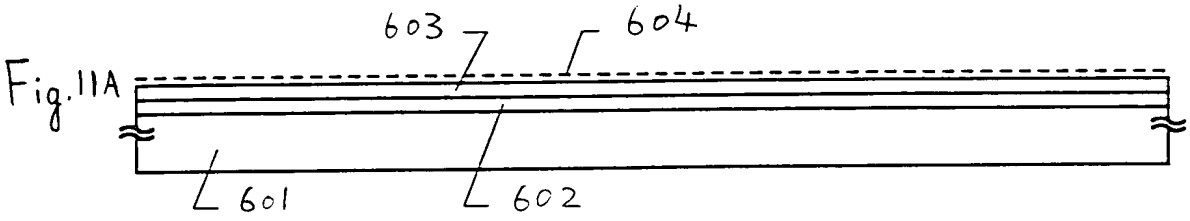


Fig.11A

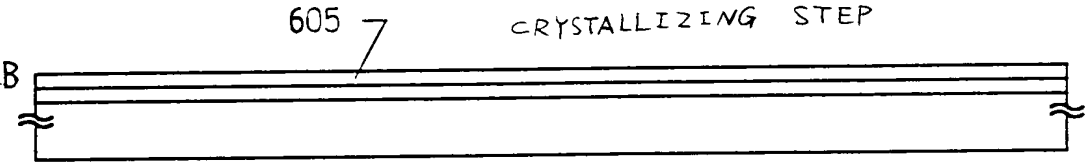


Fig.11B

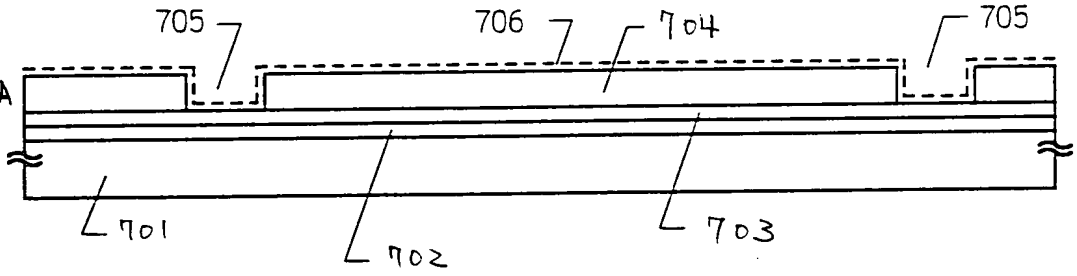


Fig.12A

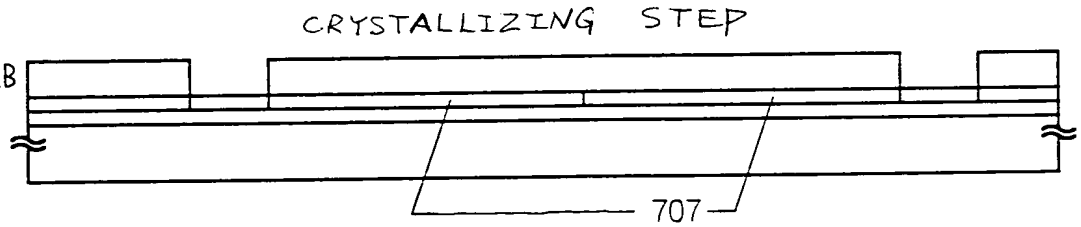


Fig.12B

PHOSPHORUS DOPING STEP

Fig.13A

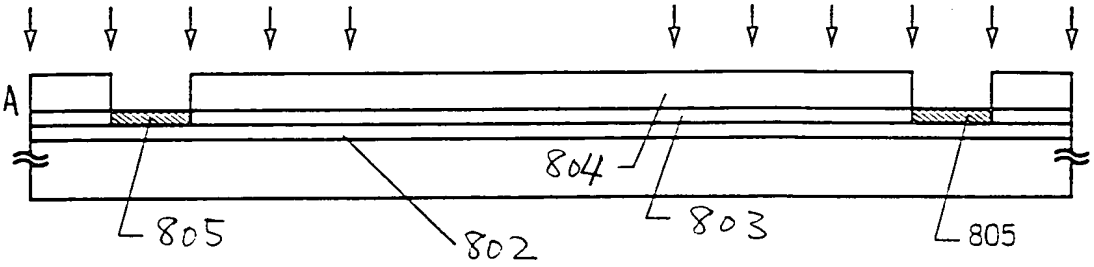


Fig.13B

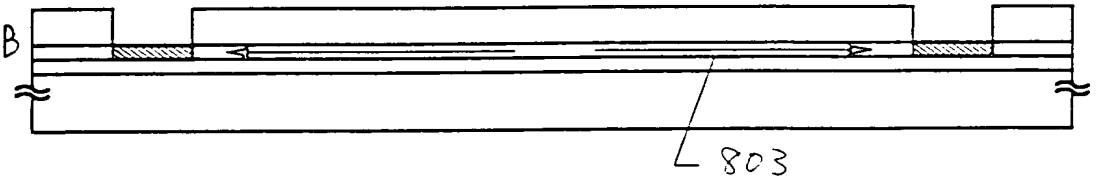
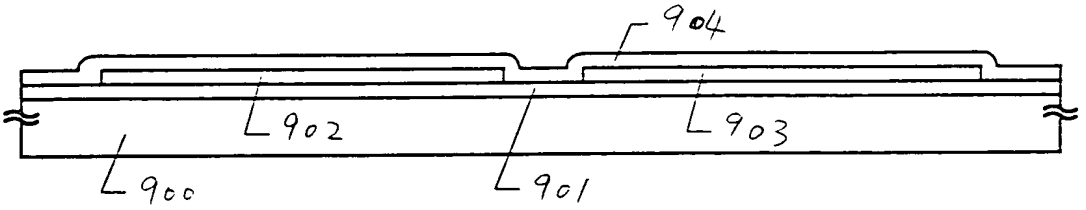
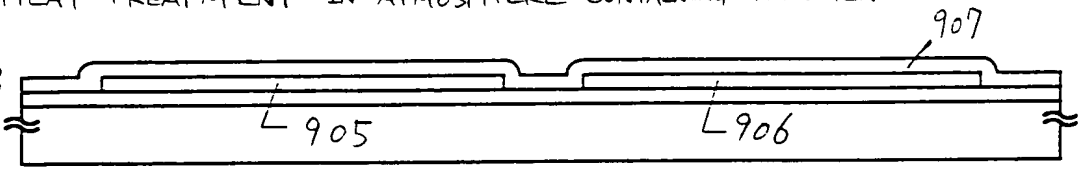


Fig.14A



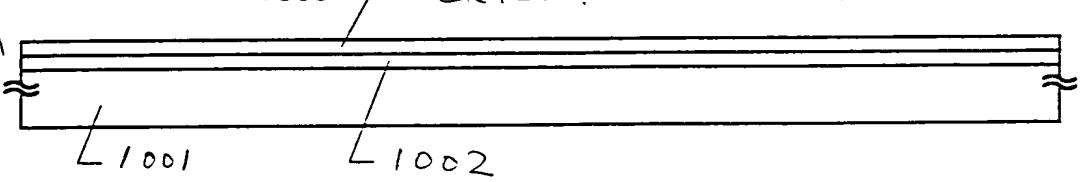
HEAT TREATMENT IN ATMOSPHERE CONTAINING HALOGEN

Fig.14B



CRYSTALLIZING STEP

Fig.15A



LOWERING TREATMENT OF IMPURITY ELEMENT BY HEATED SULFURIC ACID

Fig.15B

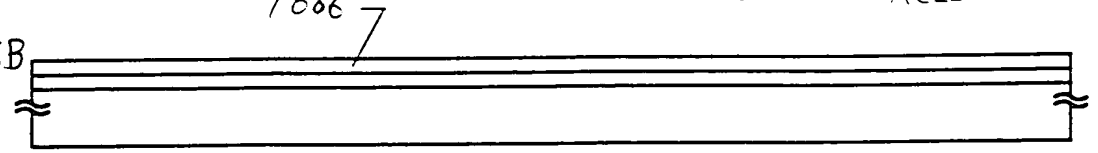
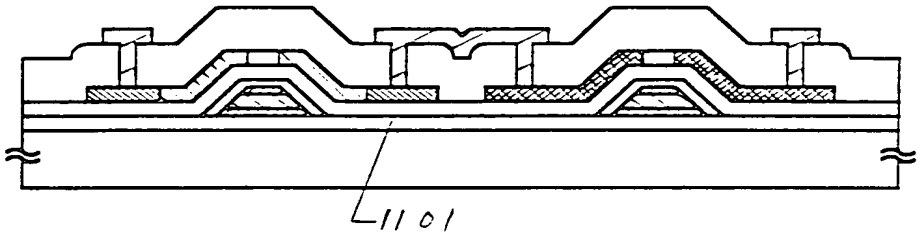


Fig. 16A REVERSE STAGGER TYPE TFT



N-CHANNEL TYPE TFT P-CHANNEL TYPE TFT

Fig. 16B FORWARD STAGGER TYPE TFT

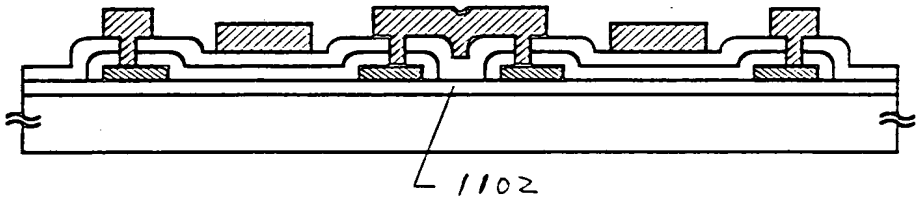
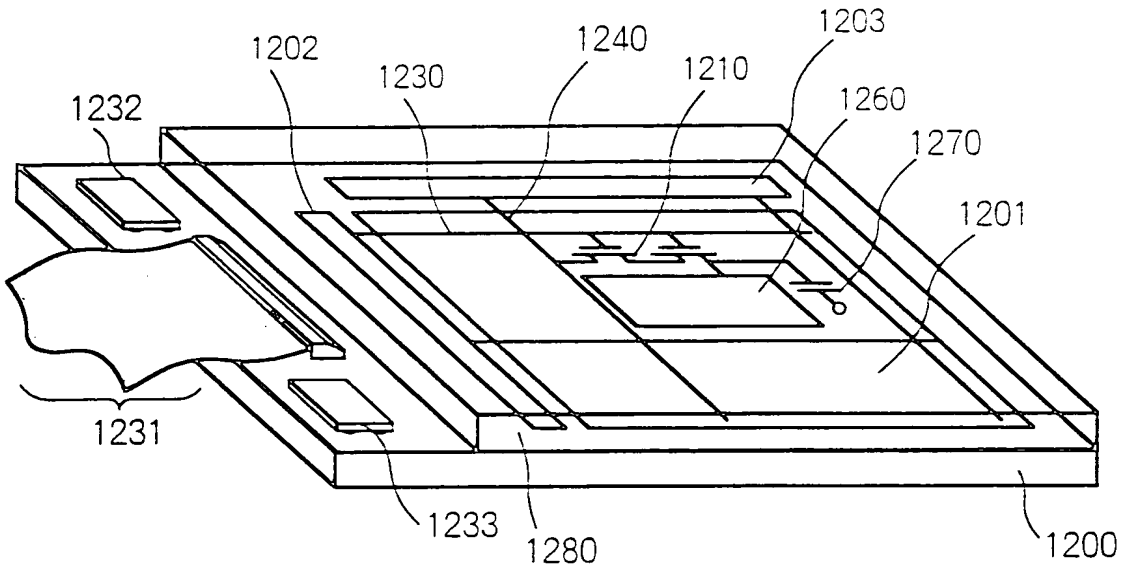


Fig. 17


1202
1230
1240
1210
1203
1260
1270
1201
1232
1231
1233
1280
1200

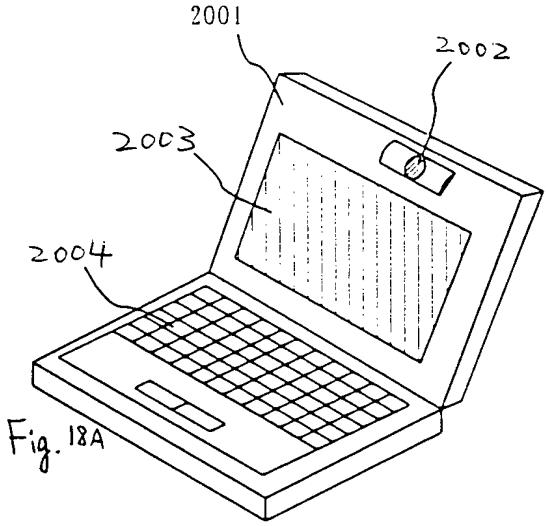


Fig. 18A

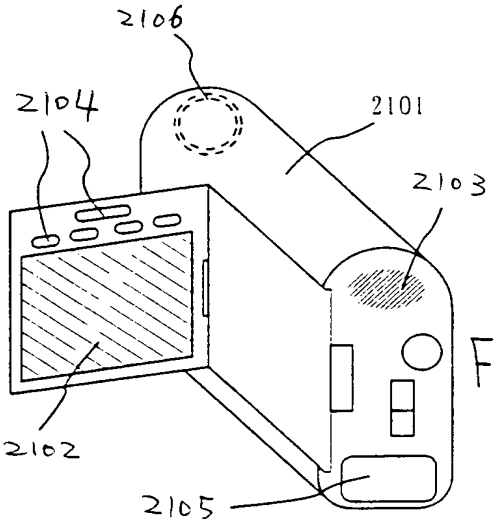


Fig. 18B

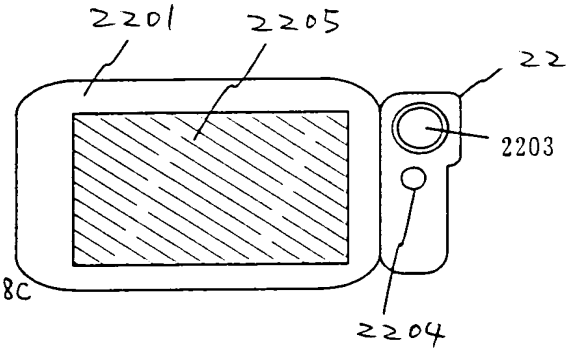


Fig. 18C

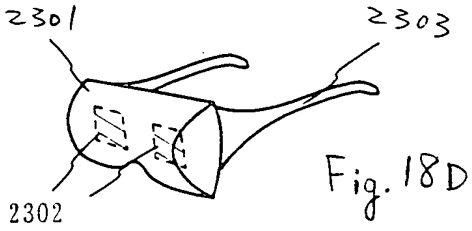


Fig. 18D

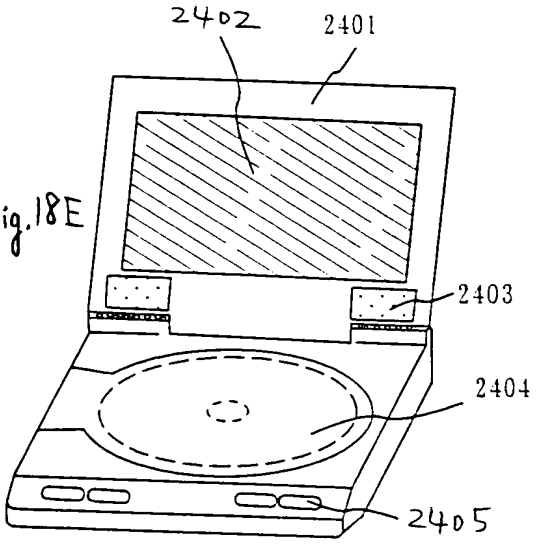


Fig. 18E

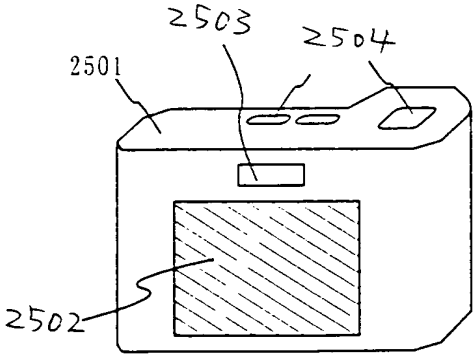


Fig. 18F

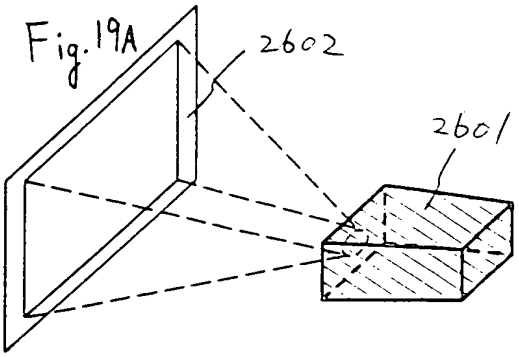


Fig. 19A

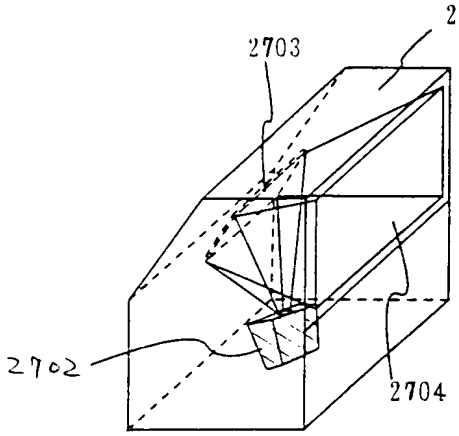


Fig. 19B

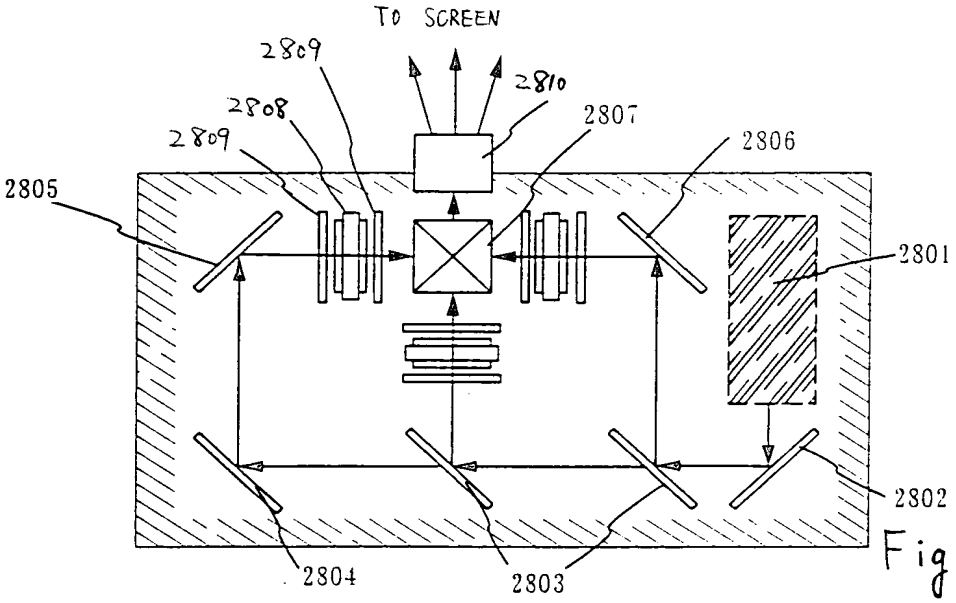


Fig. 19C PROJECTION DEVICE (THREE PLATE TYPE)

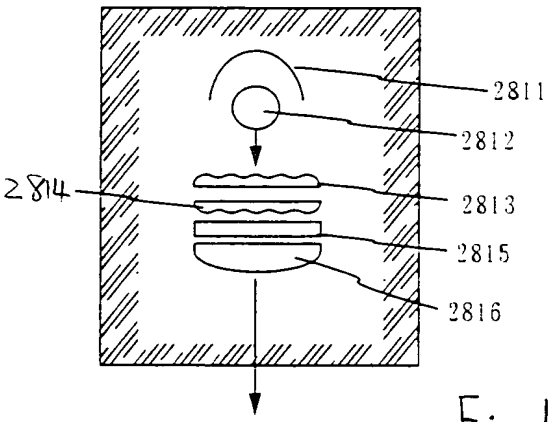


Fig. 19D LIGHT SOURCE OPTICAL SYSTEM

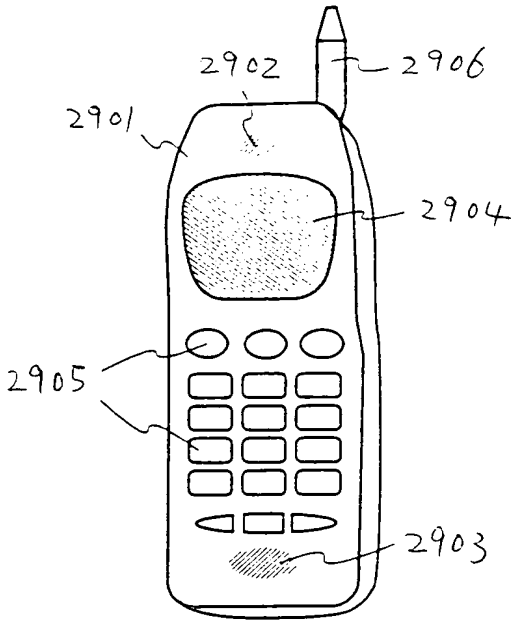


Fig. 20A

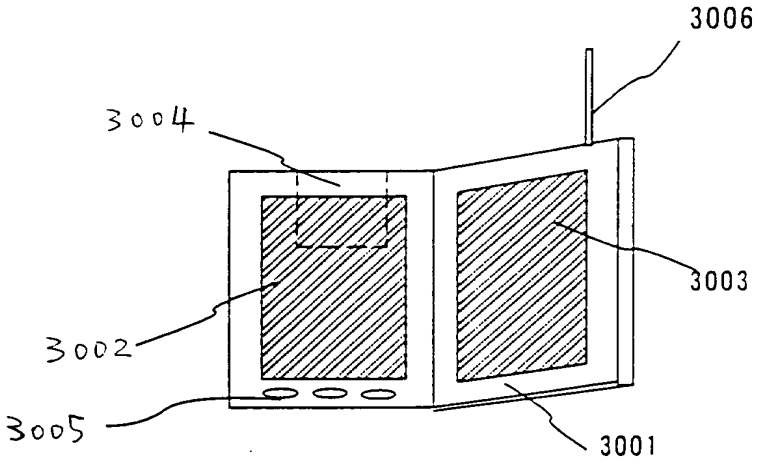


Fig. 20B

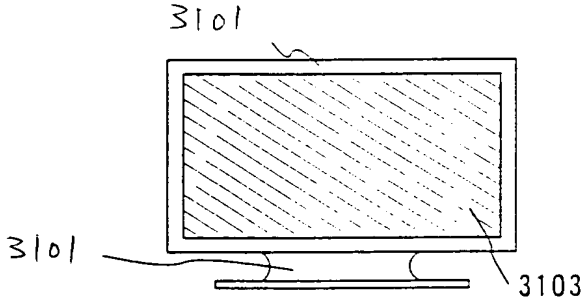


Fig. 20C

Fig. 21A

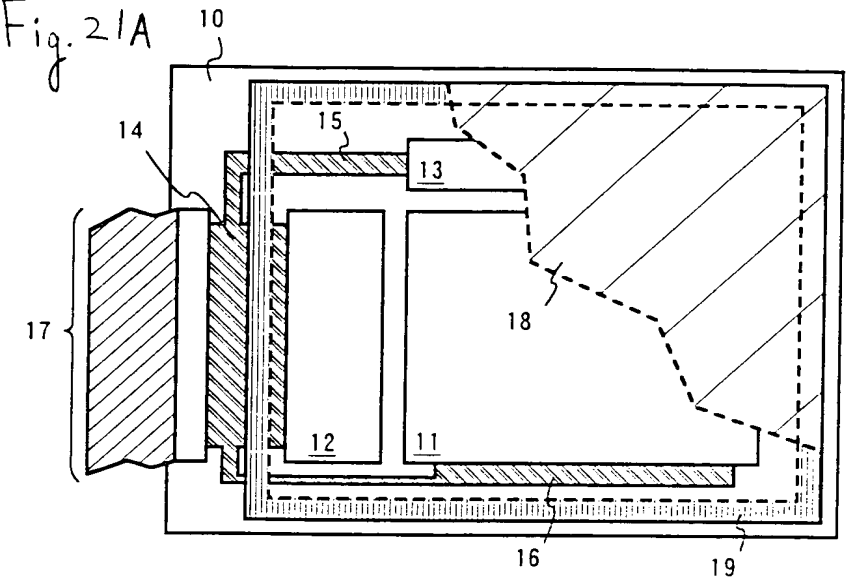


Fig. 21B

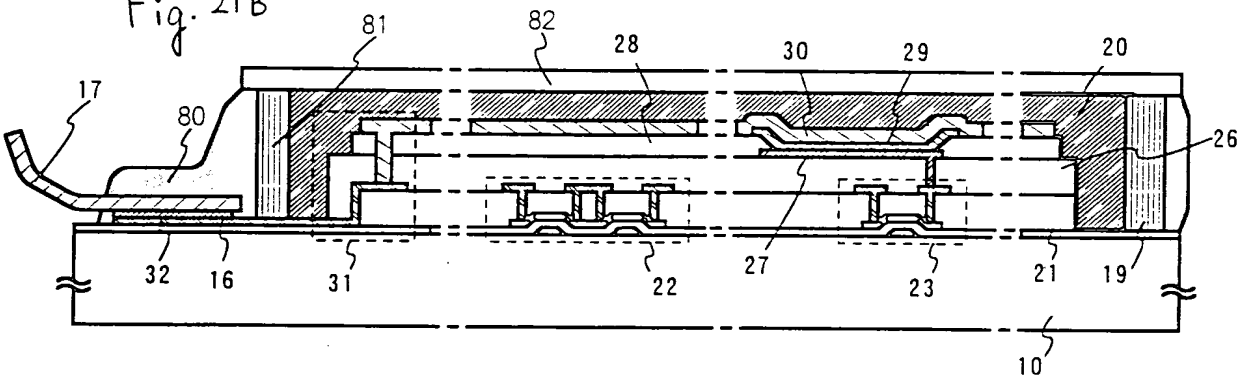


Fig. 22